

ABSTRACT OF THE DISCLOSURE

Methods for increasing defect tolerance and fault tolerance in systems
5 containing interconnected components, in which a signal level is classified as belonging
to one of a plurality of different, distinguishable classes based on one or more thresholds
separating the signal-level classes, and defect-and-fault tolerant systems embodying the
methods. An electronic-device embodiment including an array of nanowire crossbars,
the nanoscale memory elements within the nanowire crossbars addressed through
10 conventional microelectronic address lines, and a method embodiment for providing
fault-tolerant interconnection interfaces with electrically distinguishable signal levels are
described. In the described embodiment, in order to interconnect microelectronic address
lines with the nanowire crossbars within the electronic memory, an address encoding
technique is employed to generate a number of redundant, parity-check address lines to
15 supplement a minimally required set of address signal lines needed to access the
nanoscale memory elements.